

Panelists: What Needs to Happen for 3D-IC TSV Success?

It's time to get to work if we want to bring 3D-ICs with through-silicon vias (TSVs) into the semiconductor design mainstream. What ecosystem support is needed in the short term, medium term, and long term to make this new technology successful? That's the question that was put to a panel of 3D-IC experts at the recent Electronic Design Processes Symposium (EDPS) April 6, 2012 in Monterey, California. The panel was titled "The Path to the 3D Ecosystem - Short, Medium, and Long Term." It was the conclusion of a day-long session on 3D-ICs that also included user perspectives from Riko Radojic of Qualcomm and Arif Rahman of Altera; a talk by Marc Greenberg of Cadence on the wide I/O DRAM standard; and presentations by Mentor and Cadence on 3D-IC test

Open3D TSV Prototyping Program

Open 3D is fully operational for 200mm wafers now on the Minatec Campus in Grenoble, France, and will be operational in 2012 for 300mm wafers. The program is aimed at customers in a range of markets, including bio/medical, aeronautics and space, consumer applications, defense, and security, offering them enough wafers for proof of concept or prototyping. Leti said the offer is based on "limited mature technologies in order to ensure moderate costs, short cycle times and performances corresponding to the initial technical requirements of Leti customers." Open 3D operates directly on active wafers with embedded components or on passive wafers with interposer technologies.

Junctionless Silicon Nanowire Transistors for the Tunable Operation of a Highly Sensitive; Low Power Sensor (Sensors and Actuators B: Chemical)

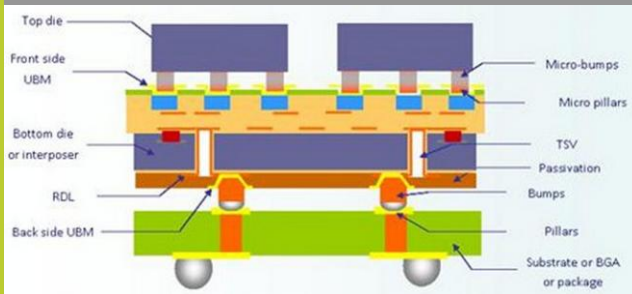
E.Buitraga, G.Fagas, M.Fernández-Bolaños Badia, Y.M.Georgiev, M.Berthomé, A. Ionescu

Highlights

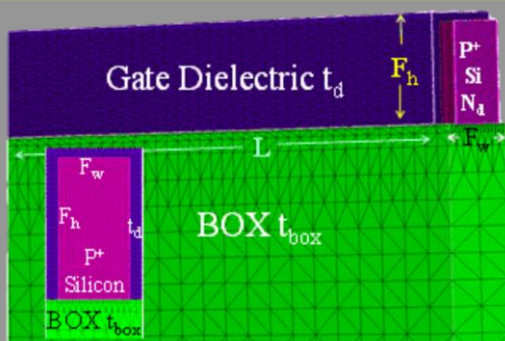
- ▶ Long channel (L 500 nm) junctionless NW/fin transistors were investigated through 3D TCAD simulations.
- ▶ Mildly doped $N_d = 1 \times 10^{19} \text{ cm}^{-3}$ structures with $F_w < 20$ nm and $\epsilon_r = 1.7$ have promising characteristics for sensors.
- ▶ These structures have $V_{th} \sim 0$ V and high relative sensitivities in the subthreshold regime $S > 95\%$.
- ▶ They also have high transconductance values at threshold $g_m, V_{fg}=0V$ 10 nS, and low subthreshold slopes $SS \sim 60$ mV/dec.
- ▶ Finally they were found to have high saturation currents $I_{d,max} \sim 1-10 \mu A$ and high I_{on}/I_{off} 104-1010 ratios.



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Open3D TSV Prototyping Program



Highly Sensitive Low Power Sensor



23rd European Symposium on Reliability of Electron Devices, Failure Physics and Analysis

October 1 - 5, 2012 Cagliari, ITALY



ESiP and e-BRAINS Workshop Experts

Joint e-BRAINS/ESiP Workshop at ESREF2012

The e-Brains Consortium jointly with the ESiP partners is organized "Heterogeneous 3D integration considered by the perspective of reliability studied in the European projects e BRAINS and ESiP" at the 23rd European Symposium on Reliability of Electron Devices, Failure Physics and Analysis on October 1, 2012 in Cagliari, Italy

ESiP Coordinator: Klaus Pressel
e-BRAINS Coordinator: Reinhard Pufall

Chair: Reinhard Pufall/ Peter Ramm

1. Reinhard Pufall
„Reliability for heterogeneous 3D integration“
2. Armin Klumpp, Peter Ramm
"Low-Temperature 3D Integration Processes for Reliable Heterogeneous Systems"
3. Maaike Taklo
„Robust design for nanostructures for optical field manipulation“
4. Alan Mathewson et al.
„Nanowire ACF for low temperature and fine pitch assembly technologies “
5. Renzo dal Molin
“Challenges of Active Medical Implants”

Chair: Klaus Pressel / H.J. Albrecht

6. Reliability and failure analysis: Challenge and differentiators for 3D-SiP An introduction into the ESiP project (by Klaus Pressel, Infineon)
7. “Heterogeneous Integration of nanowires for gas sensing applications and resulting reliability issues” (by Anton Köck, AIT, Austria)
8. “Thermal and mechanical reliability tests of plastic core solder balls” (by Maaike Visser Taklo, Sintef, Norway)
9. "Enhanced failure analysis on unfilled TSV interconnects" (by Frank Altmann/FhG IWMH and Franz Schrank /AMS Austria)
10. Acoustic microscopy for 3D-SiP failure analysis (by Peter Czurratis, PVA Tepla, Germany)
11. Reliability capability evaluation model for highly integrated packages" (by H.J. Albrecht/Siemens, Germany).
12. Implementing anti-counterfeiting technologies into IC packages – impacts & challenges in terms of reliability & failure analysis (by Stephanie Pesseguier, STMicro France)



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