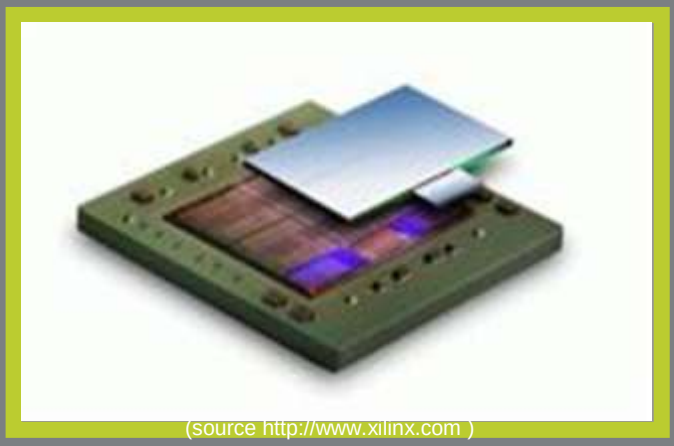
e-BRAINS Newsletter

Summer 2012 | Industry News | Issue 3



(source http://www.xilinx.com)

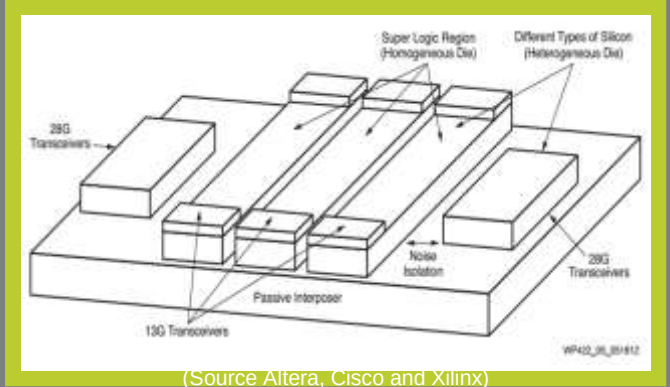
Heterogeneous 3D FPGA enables breakthrough bandwidth, signal integrity

XILINX Virtex-7 H580T FPGA is a 3D heterogeneous all programmable device that use firm's stacked silicon interconnect (SSI) technology to deliver high bandwidth, including up to sixteen 28Gbps and seventy-two 13.1 Gbps transceivers. With eight 28 Gbps transceivers and ample logic capacity, device can integrate additional line card functionality so that designers can implement a dual 100G OTN transponder on a single chip. Product support for up to four IEEE 100GE gearboxes in a single device with the option of integrating advanced debug capabilities, OTN, MAC or Interlaken IP within the same FPGA. Device is 400GE ready and will be able to support future 400GE modules that require16x25 Gbps interfaces.

(source http://www.sematech.org/)

EV Group's GEMINI® Wafer Bonding System First to Pass Equipment Maturity Assessment within SEMATECH's 3D Interconnect and Manufacturability Program

The EVG GEMINI automated wafer bonding platform is designed for meeting advanced wafer-level 3D IC integration requirements at the high-volume manufacturing level. Wafer-level 3D integration is required for applications such as DRAM or NAND flash memory stacking, heterogeneous stacking of memory onto logic devices, CMOS image sensor manufacturing and wafer-level-packaging (WLP) with TSV interconnects. Advanced wafer bonding is key for manufacturing those 3D architectures with high reliability and productivity, requiring metal bonding (Cu-Cu and Cu-Sn-Cu), fusion bonding and adhesive bonding. The EVG GEMINI systems are designed to meet all of these advanced bonding requirements at the HVM level, providing stringent process controllability, process diversity, modular design, sub-micron alignment accuracy, high throughput and reliability.
advantage of TSMC's chip-on-wafer (CoW) technology.



(Source Altera, Cisco and Xilinx)

Silicon interposers competed with TSV at ECTC

While crowds gathered for the numerous 3D through-silicon via (TSV) papers, an equal number of attendees focused on interposers – a solution that appears more near term. Papers from Altera, Cisco and Xilinx focused on product introductions and plans with silicon interposers. In an interactive session, Xilinx discussed its latest product, a 2.78Tb/s FPGA with serial connectivity – a heterogeneous solution combining three 28nm FPGA slices, two 40nm electrically isolated 28F transceiver devices, and 13G transceivers on a 65nm passive interposer (Figure 1). Cisco described a future solution featuring memory and logic on a passive interposer, while Altera's solution will take advantage of TSMC's chip-on-wafer (CoW) technology.

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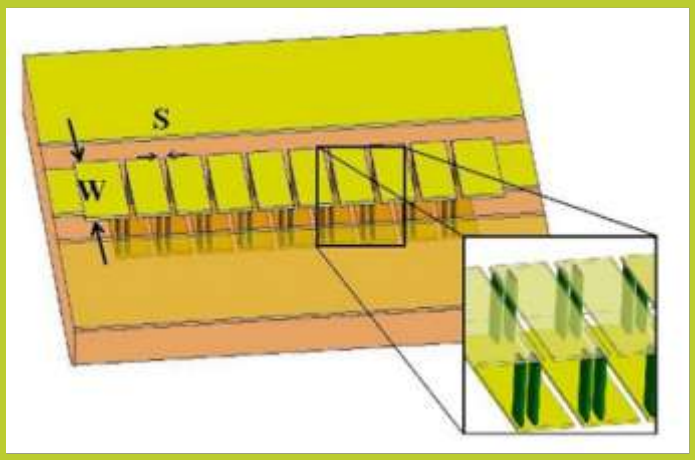

3D schematic view of the 9 turns, 2 vias series integrated inductor with a zoom in the TSV coil concept

EuroSimE 2012 in Cascais, near Lisbon, Portugal

High-Q 3D Embedded Inductors using TSV for RF MEMS Tunable Bandpass Filters (4.65-6.8 GHz)

This paper presents the optimization design of 3D integrated inductors exploiting through silicon vias (TSV) technology to improve the quality (Q) factor in the 2-20GHz range. The embedded inductor allows the heterogeneous integration with CMOS and MEMS components in a size-compact and low cost manufacturing process. Results limited to our manufacturing possibilities (5.5x15um-area tungsten TSVs, high resistivity (HR) silicon substrate) show Q-factor values as high as 35 at 8GHz for 4.8nH inductance, and design methods to improve them. These inductors are attractive to be used with MEMS capacitors for reconfigurable RFICs, as proposed for a tunable passband filter in the range 4.65-6.8GHz. The filter shows 15% continuous linear center frequency tuning and over 45% in a digital fashion. The filter is also continuously tunable in bandwidth (up to 40%) while keeping constant the center frequency.

REF: W. A. Vitale et al.; 42nd EMC, Amsterdam, Nov. 2012

EUROSIME 2012 (Lisbon)

The e-BRAINS' project partners have contributed to the 13th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems EuroSimE 2012 Lisbon, Portugal, April 16-17-18, 2012 delivering the keynote [1] and paper [2]. The EuroSimE 2012 held in Lisbon organized locally by ISQ (E. Dias Lopes) was a successful event with more than 150 registered participants.

REF:

[1] "Determination of Interface Fracture Parameters by Shear Testing Using Different Theoretical Approaches" R. Dudek 1, B. Brämer 1, J. Auersperg 1, R. Pufall 2, H. Walter 3, B. Seiler 4, B. Wunderle 5; 1 Fraunhofer ENAS, Micro Materials Center Chemnitz, Germany 2 Infineon Technologies, Munich, Germany 3 Fraunhofer IZM, Berlin, Germany 4 CWM GmbH, Chemnitz, Germany 5 TU Chemnitz, Germany

[2] "Increasing the Robustness for Reliable Packages by Prediction of Delamination by Cohesive Zone Element Simulation" R. Pufall 1, M. Goroll 1, W. Kanert 1, R. Dudek 2; 1 Infineon Technolgies AG, Neubiberg 2 Fraunhofer ENAS, Chemnitz.

Joint e-BRAINS/ESiP Workshop at ESREF2012

The e-Brains Consortium jointly with the ESiP partners is organizing "Heterogeneous 3D integration considered by the perspective of reliability studied in the European projects e-BRAINS and ESiP" at the 23rd European Symposium on Reliability of Electron Devices, Failure Physics and Analysis on October 1, 2012 in Cagliari, Italy

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